

The diagram illustrates a system architecture with the following components and connections:

- Processors:** Four **Wmt/Foster** processors (labeled **2**) are connected to the **FSB - 4**.
- Memory Controller Hub (MCH):** Labeled **6**, it contains **Re-Direction Logic** and is connected to the **FSB - 4**.
- Bus Widths:**
 - 8 bit HL_A** connects to **ICH2**.
 - 16 bit HL_B** connects to **P64H**.
 - 16 bit HL_C** (labeled **8**) connects to **P64H**.
 - AGP/PCI (or 16 bit HL_D,E)** (labeled **10**) connects to **AGP Device (or 2 P64H)** (labeled **20**).
- Intermediate Components:**
 - ICH2** (labeled **12**) contains an **IOx APIC** and connects to a **PCI Device** via a **PCI 32/33** bus.
 - P64H** (labeled **14**) contains an **IOx APIC** (labeled **16**) and connects to a **PCI Device** via a **PCI 64/66** bus (labeled **26**).
 - P64H** (labeled **18**) contains an **IOx APIC** and connects to a **PCI Device** via a **PCI 64/66** bus (labeled **22**).
 - AGP Device (or 2 P64H)** (labeled **20**) connects to a **PCI Device** via a **PCI 64/66** bus (labeled **24**).

FIG. 1

The diagram illustrates the system architecture of the Intel® Pentium® Pro. At the top, four **Wmt/Foster** processors are connected to a central **FSB** (Front Side Bus). Below the FSB is the **MCH** (Memory Controller Hub) and **Re-Direction Logic**. The MCH is connected to four different components: 1) **ICH2** (I/O Controller Hub 2) which connects to a **PCI 32/33** bus and a **PCI Device**. 2) **P64H** (Pentium Pro 64-bit Hub) which connects to a **PCI 64/66** bus and a **PCI Device**. 3) **P64H** (Pentium Pro 64-bit Hub) which connects to a **PCI 64/66** bus and a **PCI Device**. 4) **AGP Device (or 2 P64H)** which connects to an **AGP/PCI (or 16 bit HL_D,E)** bus and a **PCI Device**. The diagram also shows various buses: **8 bit HL_A**, **16 bit HL_B**, **16 bit HL_C**, and **MSI** (Memory Side Interrupt).

FIG. 2

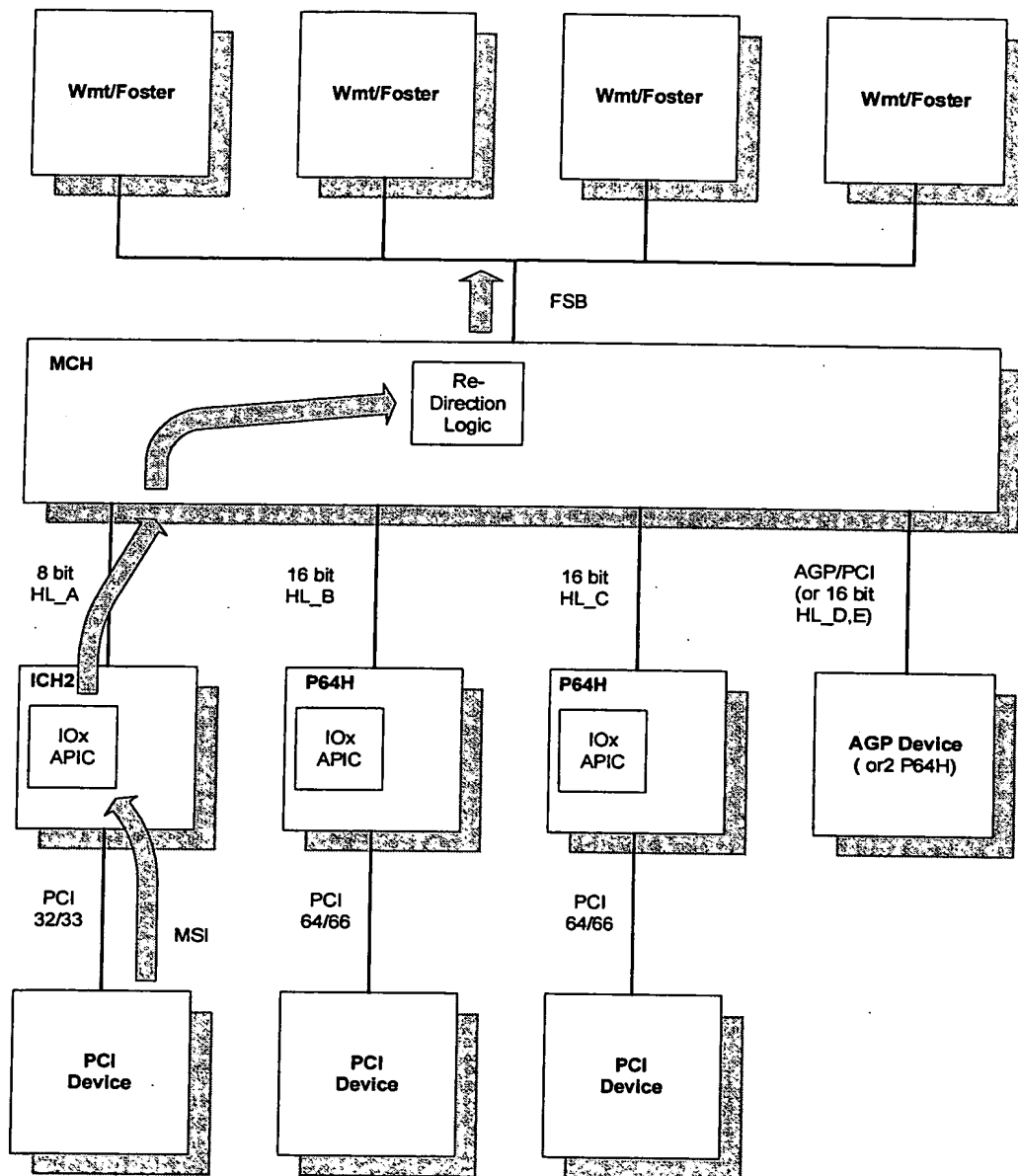


FIG. 3

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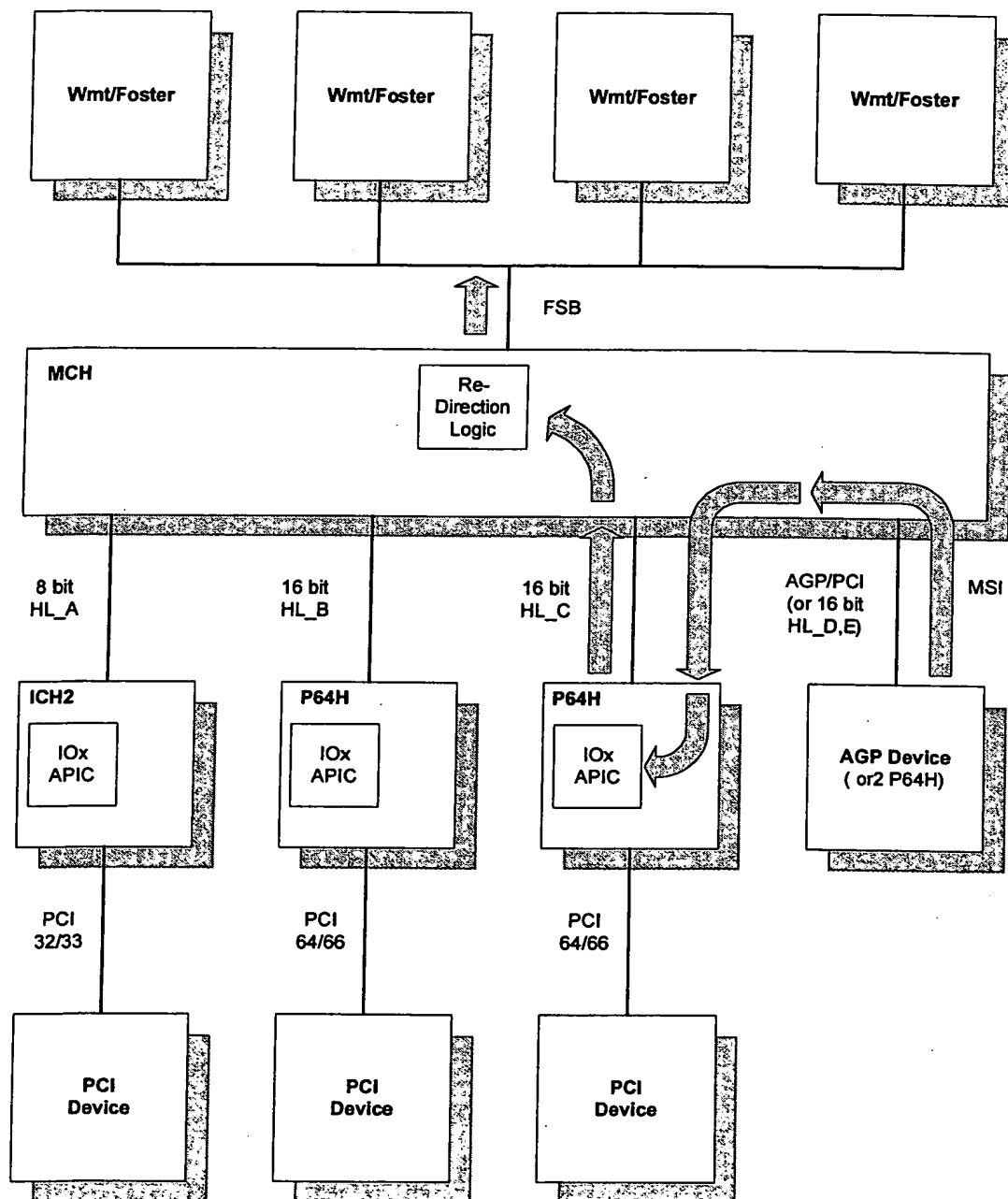
[illegible]

FIG. 4

